# Basic Calculator Implemented By MIPS Logic Operations

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*Abstract*—This write up explains the implementation of basic math operations, including addition, subtraction, multiplication and division, using the MIPS logical and normal procedures in Mars 4.5. Pictures of the code are included to help understand the program.

# I. INTRODUCTION

 $T_{\text{HE}}$  purpose of logical operators is to calculate various expressions, which is the basis of digital circuits in computer hardware. This project serves to implement a simple calculator that can perform addition, subtraction, multiplication, and division through the usage of logical operators.

The calculator that is being implemented is written using the MIPS. MIPS is a type of assembly language and the MARS software (IDE) is what is used to simulate the MIPS.

#### II. REQUIREMENTS

Section II discusses the necessary software needed to write the basic mathematical calculator and also provides the needed background information to create the calculator and understand how it works.

# A. Necessary Software's

To run MIPS assembly language, one must use the MARS software as their interactive development environment (IDE). Mars is a simulator, which acts as a runtime environment for MIPS. MARS can be downloaded on Missouri State University website as it is developed by them.

## B. Setting up the project

Go to SJSU Canvas and download the provided zip files.

# https://sjsu.instructure.com/courses/1208160/assignments/425 2547 - submit

Download the "CS47project1.zip" and unzip it. It should include the following files.

- 1. Cs47 common macro.asm
- 2. Cs47\_proj\_alu\_logical.asm
- 3. Cs47 proj alu normal.asm
- 4. Cs47\_proj\_macro.asm
- 5. Cs47 proj procs.asm
- 6. Proj-auto-test.asm

Open the Mars 4\_5 jar file downloaded from the Missouri state university webpage. Go to "File" and click on "open".

Find your way to the directory, which contains the unzipped files. Since MARS does not allow you to load all the files at

once, load each of them separately. After all the files have been loaded and opened, MARS should look like this.

Edit Execute					
cs47_common_macro.asm	CS47_proj_alu_logical.asm	CS47_proj_alu_normal.asm* cs47_proj_macro.asm			
C347_CONINION_INACIO.asin					

Fig.1. Opening/loading files onto MARS

C. Boolean Algebra/logic

Implemented circuitry in computer hardware systems requires a deep understanding of Boolean logic and algebra. In circuits, only the numbers 1 and 0 exists, nothing else. One must use truth tables to find out the output of a Boolean expression.

Here is an example of the AND Boolean operation where t represents a T and 0 represents a F. AND is the multiplication of two values.

	Table 1	1:	Truth	Table	for	Logical	AND
--	---------	----	-------	-------	-----	---------	-----

А	В	A.B
0	0	0
0	1	0
1	0	0
1	1	1

In addition to the AND operation, there exists an OR operation. OR is used for addition of two binary integers in Boolean algebra. The OR operation returns 0 if both A and B are 0. The following is the truth table of Logical OR.

Table 2: Truth Table for Logical OR

А	В	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Finally, there exists an XOR operation, which means exclusive OR. XOR returns 0 if both A and B are either 0 or 1. The XOR operation returns 1 if only one of the two is 1.

Table 3: Truth Table for Logical XOR

А	В	A.B
0	0	1
0	1	1
1	0	1
1	1	0

# D. Binary

Binary is a number system with base 2, unlike the decimal system, which uses base 10. Since this system is base 2, it consists of only 2 symbols that can be used, 0 or 1. For example, if we used a 4 bit long word, 0 is represented as 0000 and 1 is represented as 0001. Once a digit reaches 1, it becomes 0 and rolls over to the next larger digit and places a 1 there. Thus, 2 would be represented as 0010. The binary system is extremely useful when it comes to computers as a computer system can only read 1's and 0's.

Now the question is, how does one represent a negative number in binary? This is where the "two's compliment" form comes into play. In two's compliment, if a 1 exists in the MSB position, that means the number is negative. If a 0 exists in the MSB position, then the number is positive. For example, 3 in twos compliment is 0011, where as -3 is 1101. To obtain the negative of a number, inverse all the bits of the positive number and add 1. If we inverse all the bits of +3, we get 1100. Add 1 to this, and we obtain 1101, which is -3.

#### **III. DESIGN AND IMPLEMENTATION**

Section 3 discusses the design of the arithmetic calculator and how it's being implemented in MIPS. This calculator implements addition, subtraction, multiplication, and division operations.

#### A. Design

The design section talks about the design of the addition, subtraction, multiplication, and division operations.

# 1) Addition and subtraction

Addition and subtraction both relate in the sense that subtraction is the addition of the negation of the second integer. For example, A-B = A + (-B). For the addition operation, a full adder must be implemented since the carry bit has to be taken into consideration. A half adder can only add two bits.

The way addition works is a carry bit starts off as 0 and is added with the LSB bits of the two inputs. The sum is put into the LSB position of the answer, and the carry bit is found and added to the next two bits of the inputs. To get the nth digit, the logical XOR is called on the first bits and is stored. Then, the logical XOR is called on the stored value and the carry in. This results in the sum bit and is stored temporarily. To find the carry bit, first initialize the carry bit to 0. To find the carry bit, first we use the XOR operation on the two inputs and store it in lets say \$t7. AND is called on \$t7 and the initial carry bit (v1) and is stored in \$t8. Then, AND is used on the nth bits of the two inputs. Finally, OR is called on \$t8 and \$t1 and is stored back in the carry bit register which is \$v1.

These operations are performed 32 times, since there are 32 bits in each register. Finally, the sum of the two inputs will be calculated.

For subtraction, the only change that must be made is the complement of the second input must be taken. Then pass the first input and the complement of the second input into the add loop and the difference (in this case a sum) will be calculated.

# 2) Multiplication

For unsigned multiplication, a counter (\$t0) is initially set to 0. The first input, which is the multiplicand, is saved in a temporary register (\$t4). The second input, which is the multiplier, is put into a temporary register (\$t1). This represents the lo of the multiplication. The high is initially set to 0 and put into temporary register \$t2.

In short, binary multiplication is simply repeated addition. What we must know is that  $0 \ge 0$ ,  $1 \ge 0$ ,  $1 \ge 0$ , and  $1 \ge 1$ . If the current bit of the multiplier is 0, then 0 gets placed in that bit position of the answer. If the multiplier is 1, then simply put the multiplicand into that bit position of the answer.

#### 3) Division

First, we must align the divisor with the MSB bits of the dividend. Compare these bits to the divisor. If these bits are greater than the divisor, the quotient bit is set to 1 and then subtraction is performed with MSB bits – divisor. If the MSB bits are less than the divisor, the quotient bit is set to 0 and subtraction is not performed. The divisor is then shifted one bit to the right and we compare the MSB bits to the divisor again. This continues until division is over.

#### B. Implementation

To implement the calculator operations, many macros and utility procedures are designed to help make the implementation easier.

#### 1) Utility Macros

The 4 macros created are extract\_nth\_bit, insert\_to\_nth\_bit, store\_stack\_all, and restore\_stack\_all.

# *i. Extract\_nth\_bit* The extract\_nth\_bit macro obtains a bit value at a given position for any integer.

The macro contains three arguments passed in as regD, regS, regT. regD is the destination register where the result will be stored. regS is the source register which contains the bit pattern which the calculator will be extracting from. regT holds the position of the bit that will be extracted.

First, \$regS is moved into \$s0 just so that the original source register does not get messed up. Then, \$s0 is shifted right by the bit position number and is stored back into \$s0. Finally, AND is used on \$s0 and 1 to extract the bit and is put into the destination register. Basically, if \$s0 is 0x0, AND'ing it with 1 will result in 0. If \$s0, is 0x1, AND'ing it with 1 will result in 1. This properly extracts the needed bit.

ii. Insert to nth bit

The insert\_to\_nth\_bit macro inserts a given bit into the nth position of a bit pattern and returns the bit pattern.

<pre>.macro insert_one_to_nth_bit(\$regD, \$re</pre>	gS, \$regT, \$maskReg)
li \$maskReg, 1	
<pre>sllv \$maskReg, \$maskReg, \$regS</pre>	
<pre>not \$maskReg, \$maskReg</pre>	
and \$regD, \$maskReg, \$regD	#forces 0 in to the position where you want to inse
<pre>sllv \$regT, \$regT, \$regS</pre>	
or \$regD, \$regD, \$regT	<pre>#regD is the register with the inserted information</pre>
.end_macro	

The macro contains four arguments passed in as regD, regS, regT, and maskReg. regD contains the bit pattern in which the proper bit will be inserted into. regS contains the insertion position. regT contains what bit will be inserted, either a 1 or 0. Finally, maskReg is any temporary register in which a mask will be created.

Initially the mask register is set to 1 and is then shifted left by the regS amount, which is the insertion position. All of the bits in the mask register are then inverted by using the NOT operation. Next, AND is used on the mask register and the bit pattern in which we are inserting to force 0 into the position in which we are inserting. regT, which contains the bit to be inserted is then shifted left by the regS amount to get into the right position. Finally, or is used on regD and regT to finish the insertion process.

*iii.* Store\_stack\_all and restore\_stack\_all These two macros serve to store and restore registers \$fp, \$ra, \$a0-\$a3 and \$s0-\$s7. Unlike the other macros, these macros don't take in any arguments.

<pre>.macro store_st</pre>	tack_all
#store	RTE - 5 *4 = 20 bytes
addi	\$sp, \$sp, -60
SW	\$fp, 60(\$sp)
SW	<pre>\$ra, 56(\$sp)</pre>
SW	\$a0, 52(\$sp)
SW	\$a1, 48(\$sp)
SW	\$a2, 44(\$sp)
SW	\$a3, 40(\$sp)
SW	\$s0, 36(\$sp)
SW	\$s1, 32(\$sp)
SW	\$s2, 28(\$sp)
SW	\$s3, 24(\$sp)
SW	\$s4, 20(\$sp)
SW	\$s5, 16(\$sp)
SW	\$s6, 12(\$sp)
SW	\$s7, 8(\$sp)
addi	\$fp, \$sp, 60
.end macro	

.end\_macro

macro	restore	stack	all	
	_		5 *4 = 20 bytes	
	lw	\$fp,	60( <mark>\$sp</mark> )	
	lw	\$ra,	56( <mark>\$sp</mark> )	
	lw	\$a0,	52(\$sp)	
	lw	\$a1,	48( <mark>\$sp</mark> )	
	lw	\$a2,	44( <mark>\$sp</mark> )	
	lw	\$a3,	40( <mark>\$sp</mark> )	
	lw	\$s0,	36( <mark>\$sp</mark> )	
	lw	\$s1,	32(\$sp)	
	lw	\$s2,	28( <mark>\$sp</mark> )	
	lw	\$s3,	24( <mark>\$sp</mark> )	
	lw	\$s4,	20( <mark>\$sp</mark> )	
	lw	\$s5,	16( <mark>\$sp</mark> )	
	lw	\$s6,	12( <mark>\$sp</mark> )	
	lw	\$s7,	8(\$sp)	
	addi	\$sp,	\$sp, 60	
	jr \$ra			

.end\_macro

Although it is not necessary to always store and restore these registers, these macros still do it regardless.

#### 2) Utility Procedures

*i. twos\_complement* 

An argument a0 is passed into the twos\_complement subroutine and the complement of the argument is returned in the v0 register.

In the twos\_complement subroutine, the NOT of \$a0 is taken and stored back in \$a0. The number 1 is then put into \$a1 and both \$a0 and \$a1 are passed into the add\_loop method. This way, the complement of \$a0 is taken.

```
twos_compliment:
       not $a0, $a0
       li $a1, 1
       addi
                $sp, $sp, -16
       SW
                $fp, 16($sp)
       SW
                $ra, 12($sp)
       SW
                $t0, 8($sp)
       addi
               $fp, $sp, 16
       li $t0, 0
                        # counter set to 0
       li $v1, 0
                        #carry bit initially set to 0.
                        #always pick 0 from extract routine b
       li $t3, 0
       li $v0, 0
                        #final sum
       jal add_loop
       lw
                $fp, 16($sp)
                $ra, 12($sp)
       lw
                $t0, 8($sp)
       1w
       addi
                $sp, $sp, 16
       ir $ra
```

ii. Twos\_complement\_if\_neg

Twos\_complement\_if\_neg branches to twos\_complement if the argument is less than 0, or returns the argument itself if it is above 0.

twos\_compliment\_if\_neg: bltz \$a0, twos\_compliment la \$v0, (\$a0) jr \$ra

# *iii. Twos\_complement\_64bit*

Twos\_complement\_64bit returns the complement of the lo and hi of the multiplied result. The lo exists in the \$a0 register and the hi exists in the \$a1 register.

\$a0 and \$a0 are inverted using not. \$a1 is then saved in \$a3 and 1 is loaded into \$a1. Add\_loop is then called on \$a0 and \$a1, which is the lo and 1 respectively. Once add\_loop is done, twos\_complement\_64bit is returned to and the answer (\$v0) is stored in \$t0. The carry bit (\$v1) is saved in \$a1 and \$a3 is moved back into \$a0. Add\_loop is then called again with the new \$a0 and \$a1. After this, the twos complement 64bit is done.

```
twos_compliment_64bit:
        addi
               $sp, $sp, -12
                $fp, 12($sp)
        SW
               $ra, 8($sp)
                                #store return address
        SW
       addi
               $fp, $sp, 12
       not $a0, $a0
                        #a0 contains lo half of multiplie
       not $a1, $a1
                        #al contains hi part of multiplie
        la $a3, ($a1)
                        #saving hi half into a3
        li $a1, 1
                        #loading 1 into a1
        li $t0, 0
                        # counter set to 0
        li $v1, 0
                        #carry bit initially set to 0.
        li $v0, 0
                        #final sum
       jal add_loop
        la $t3, ($v0)
        la $a1, ($v1)
        la $a0, ($a3)
        li $t0, 0
                        # counter set to 0
                        #carry bit initially set to 0.
        li $v1, 0
        li $v0. 0
                        #final sum
       jal add_loop
                $fp, 12($sp)
        1w
                $ra, 8($sp)
               $sp. $sp. 12
       addi
             la $v1, ($v0)
             la $v0, ($t3)
```

#### *iv. bit replicator and replicate*

jr \$ra

These two procedures replicate bits of a given register. Bit\_replicator checks if the argument is 0, and if it is, branches to replicate\_zero. Replicate\_zero will load 0 into \$v0 and returns back to the caller address. If bit\_replicator doesn't branch, -1 is loaded into \$v0 and returns back to the caller address.

```
bit_replicator:
    beqz $a0, replicate_zero
    li $v0, 0xFFFFFFF
    jr $ra
replicate_zero:
    li $v0, 0
    jr $ra
```

3) Addition/subtraction implementation

```
addition_au_logical:
                           # counter set to Ø
            li $t0, 0
            li $v1, 0
                           #carry bit initially set to 0.
            li $v0, 0
                           #final sum
            jal add_loop
                    $fp, 20($sp)
            lw
            lw
                    $ra, 16($sp)
            lw
                    $a0, 12($sp)
                    $a1, 8($sp)
            lw
            addi
                    $sp, $sp, 20
            restore_stack_all
            #jr $ra
    subtraction_au_logical:
            la $t0, ($a0)
            la $a0, ($a1)
            jal twos_compliment
            la $a1, ($v0)
            la $a0, ($t0)
            j addition_au_logical
add_loop: #registers used: $t0, $t1, $t2, $t4, $t5, $t6, $
        li $t4, 32
        beq $t0, $t4, done
                                          #if the counter (to
        extract_nth_bit($t5,$a0, $t0)
                                         #extract nth bit o
        extract_nth_bit($t6,$a1, $t0)
                                         #extract nth bit o
        xor $t7, $t5, $t6
        xor $t2, $t7, $v1
                                  # sum bit calculated, xor
        and $t8, $t7, $v1
                                 #partial carry out
                                 # and of bit n of A and bu
        and $t1, $t5, $t6
        or $v1, $t8, $t1
                                  #final carry bit
        insert_one_to_nth_bit($v0, $t0, $t2, $t9)
        addi $t0, $t0, 1
                                  #increment counter by 1
        j add loop
# TBD: Complete it
done:
        jr $ra #restore_stack_all
```

Addition\_au\_logical sets up the addition process. It creates the necessary variables and jumps to the add\_loop. For subtraction\_au\_logical, the second input is moved into a0, and the twos complement is taken. Then all the variables are stored back in their correct position and the method jumps to addition\_au\_logical.

Add\_loop is where the addition actually takes place. This loop calculates the sum of the \$a0 and \$a1 registers. The method first sets a register to the immediate value of 32 so that the loop has a value to compare to. The loop checks if the counter is equal to 32. If it is, it branches to "done" and returns to the caller. If it does not equal 32, the loop is executed. The nth bits of the two inputs are extracted and stored in \$t5 and \$t6 respectively. XOR is used to calculated the sum bit and AND/OR are used to calculate the final carry out bit. The sum bit is then inserted into the correct position of the final answer (\$v0) and the counter is then incremented by 1. The procedure then jumps back to itself. 3) Multiplication implementation multiplication\_au\_logical: la \$a3, (\$a1) #saving al into a3 jal twos\_compliment\_if\_neg la \$t0, (\$v0) #2's compliment of a0 (mcnd) la \$a0, (\$a3) jal twos\_compliment\_if\_neg #get 2's compl. la \$a1, (\$v0) la \$a0, (\$t0) j mul\_unsigned mul\_unsigned: #a0 = mcnd, a1 = mplr li \$t0, 0 #counter la \$t1, (\$a1) #lo (l) li \$t2, 0 #hi (h) la \$t4, (\$a0) #save mcnd extract beginning: extract\_nth\_bit(\$a0, \$t1, \$zero) #a0 gets the Oth jal bit\_replicator #v0 gets the replicated bit, whic and \$t5, \$t4, \$v0 la \$a0, (\$t2) #move old h value into a0 #move the 0 or mcnd (t5) into al la \$a1, (\$t5) #now add old H with mcnd or 0, depending on what the Oth addi \$sp. \$sp. -44 \$fp, 44(\$sp) SW \$ra, 40(\$sp) SW sw \$t0, 36(\$sp) \$t1, 32(\$sp) SW \$t2, 28(\$sp) SW \$t3, 24(\$sp) sw \$t4, 20(\$sp) sw sw \$t5, 16(\$sp) \$a0, 12(\$sp) sw \$a1, 8(\$sp) SW addi \$fp, \$sp, 44 li \$t0, 0 # counter set to 0 li \$v1, 0 #carry bit initially set to 0. li \$v0. 0 #final sum jal add\_loop \$fp, 44(\$sp) lw \$ra, 40(\$sp) lw lw \$t0, 36(\$sp) lw \$t1, 32(\$sp) lw \$t2, 28(\$sp) lw \$t3, 24(\$sp) lw \$t4, 20(\$sp) lw \$t5, 16(\$sp) lw \$a0, 12(\$sp) \$a1, 8(\$sp) lw addi \$sp, \$sp, 44 la \$t2, (v0) #h = h + x #next part is shifting 64 bits to the right srl \$t1, \$t1, 1 #shift mplr right by 1 bit extract\_nth\_bit(\$t7, \$t2, \$zero) #extracting bit ( li \$t8. 31 insert\_one\_to\_nth\_bit(\$t1, \$t8, \$t7, \$t9) #move bit 0 of #shift hi right by 1 bit srl \$t2, \$t2, 1 addi \$t0, \$t0, 1 #increment loop counter i li \$t8, 32 beq \$t0, \$t8, done\_mult #auit of counter = 32 j extract\_beginning

```
done_mult:
         la $v0, ($t1)
                           #this moves the lo, 32 bit result, into v0
         la $v1, ($t2)
                           #this moves the hi, 32 bit result, into v1
         l.
                   $fp, 20($sp)
         lw
                  $ra, 16($sp)
         lw
                  $a0, 12($sp)
         lw
                   $a1, 8($sp)
         addi
                  $sp, $sp, 20
         #restore stack all
         li $t8, 31
         extract_nth_bit($t1, $a0, $t8) #extract bit 31 of a0
extract_nth_bit($t2, $a1, $t8) #extract bit 31 of a1
         xor $t6, $t1, $t2
                                     #if xor is 1, that means only one number is
         beqz $t6, positive
la $a0, ($v0)
         la $a1, ($v1)
         jal twos compliment 64bit
         restore stack all
         #jr $ra
positive:
         restore_stack_all
                                     #restore will take u to caller
         #jr $ra
```

*i.* Multiplication au logical

Multiplication\_au\_logical sets up the entire

multiplication process. It first checks to see if both number are negative by using twos\_complement\_if\_neg, then jumps to mul\_unsigned.

Mul\_unsigned gets all the necessary registers needed for storage and continues on to extract\_beginning. Extract\_beginning first gets the 0<sup>th</sup> bit of the lo and stores it in \$a0. \$a0 is then replicated using bit\_replicator and is stored in \$v0. AND is then called on the replicated bit pattern and \$t4, which holds \$a0 (MCND). Now we want to add the original Hi with the mcnd or 0, depending on what the 0<sup>th</sup> bit was, and the value is stored back into the register, which holds the Hi. Next, the Lo is shifted right by 1 bit and the 31<sup>st</sup> bit of Lo gets the 0<sup>th</sup> bit of the Hi. Then, the Hi is shifted right by 1 bit and the counter is incremented by 1. Next, we check if the counter equals 32, and if it does, that means all the multiplicating is over and we jump to "done\_mult". If it does not equal 32, we jump back to the "extract beginning".

#### ii. done mult

Done\_mult begins with storing the lo (1) into 0 and storing the hi (1) into 1. Next, the code finds out if one of the initial inputs were negative or if both are either positive or negative. We check to see if both are negative or if both are positive by calling an XOR on the  $31^{st}$  bit of each number. If the XOR is equal to 1, that means only one of the inputs is negative, meaning that the sign bit should be negative. If the XOR is 0, we branch to "positive" which restores the stack and jumps back to the caller. If the code does not jump to positive, twos complement 64 bit is called on hi and lo and then the stack is restored and returned back to the caller.

```
Division implementation
4)
      division_au_logical: #start of division_au_logical
    la $a3, ($a1) #saving a1 into a3 (start of division_au_logical)
                  jal twos_compliment_if_neg
                                       #2's compliment of a0 (mcnd)
                     $t0, ($v0)
                  la $a0, ($a3)
                  jal twos_compliment_if_neg
                                                                #get 2's compliment of mplr if needed
                 la $a1, ($v0)
la $a0, ($t0)
                 j div_unsigned
      div_unsigned: #start of unsigned division
                  instance of ansigned aivision
fund, al is dvsr, s0 is I; s3 is R; s1 is Q and DVND;
li $s7, 0 #counter set to 1
                 li $s7, 0 #counter set to 1
la $s1, ($a0) #dvnd put in s1 (Q)
la $s2, ($a1) #dvsr put in s2 (D)
      li $s3,0 #remaind
#li $s4,31 #needed
#start of left shit and extract
                                         #remainder set to 0 (R)
                                         #needed to extract 31 bit of quotient
      left_shift_and_extract:
                 li $$4, 31 #needed to extract 31 bit of quotient
sll $$3, $$3, 1 #shift remainder by 1 to the left
extract_nth_bit($$5, $$1, $$4) #extract the 31st bit of the quotient (t1
                  insert_one_to_nth_bit($s3, $zero, $s5, $s6)
                                                                                       #insert t5 at the Oth pos
      sll $s1, $s1, 1 #shift left the quotient by 1
la $a0, ($s3) #set a0 to the remainder
la $a1, ($s2) #set a1 as dvsr (D)
             #part of sub logical and addition au logical
```

```
la $t0, ($a0)
la $a0, ($a1)
        jal twos_compliment
        la $a1, ($v0)
la $a0, ($t0)
        li $t0, 0
                         # counter set to 0
                         #carry bit initially set to 0.
        li $v1, 0
                         #final sum
        li $v0, 0
        jal add_loop
                         #after this, v0 will contain S. Doing S = R-D
        bltz $v0, increment_counter
        la $s3, ($v0)
                        #putting s into r
        li $t0, 1
        insert_one_to_nth_bit($s1, $zero, $t0, $v1) #insert 1 at q[0].
#start of increment counter
increment counter:
        li $s4, 32
        addi $s7, $s7, 1
        beq $s7, $s4, end_division
        j left_shift_and_extract
 #end division
 end division:
         la $v0. ($s1) #moving 0 into v0
         #pop the a0 and a1 since we added it at the very beginning
                 $fp, 20($sp)
         lw
         lw
                 $ra. 16($sp)
                 $a0, 12($sp)
         lw
         lw
                 $a1, 8($sp)
         addi
                 $sp, $sp, 20
         la $s6, ($a0)
                        #temp store the original dvnd
         la $s7, ($a1) #temp store the original dvsr
         #restore stack all
         li $t8. 31
         extract_nth_bit($t1, $a0, $t8) #extract bit 31 of a0
         extract_nth_bit($t2, $a1, $t8) #extract bit 31 of a1
                                 #if xor is 1, that means only one number
         xor $t6, $t1, $t2
         begz $t6, positive_div
         la $a0, ($s1)
                                 #load gutoeint into a0
                                 #find twos of quotient, answer is put it
         ial twos compliment
          la $s1, ($v0) #temp store the twos compliment of the quotient i.
         la $a0, ($s3)
                         #move remainder to a0
         #check if divisor is negative, so msb is 1. is divisor is negative
         li $t8, 31
         #la $a1. ($s7)
         extract_nth_bit($t1, $s7, $t8) #extract bit 31 of a0
         batz $t1. skip secondtwos
```

```
la $v1, ($v0) #move twos compliment of remainder
                       #2's complement of quotient goes in
       la $v0, ($s1)
       restore_stack_all
skip secondtwos:
        la $v0, ($s1)
                       #move twos compliment of quotient b.
                       #move remainder back into v1
        la $v1, ($s3)
       restore_stack_all
positive_div:
        la $s5, ($v0)
                       #save original O
        la $v1, ($s3)
                      #moving remainder into v1
        #check if s7 is negative
       li $t8, 31
       extract_nth_bit($t1, $s7, $t8) #extract bit 31 of .
       beqz $t1, restore
```

```
i) Division au logical
```

jal twos\_compliment

la \$a0, (\$v1)

la \$v1, (\$v0) la \$v0, (\$s5)

jal twos\_compliment

Division\_au\_logical obtains the twos complement of the two inputs if they are below 0. Then the method jumps to div\_unsigned.

#### ii) div\_unsigned

Div\_unsigned begins by setting up the proper arguments as variables. A counter, \$s7, is initialized to 0. \$s0, which holds the Quotient, is set to \$s1. \$a1, which holds the dvsr, is set to \$s2. And finally \$s3, which is the remainder, is set to 0.

#### *iii) left shift and extract*

In left\_shift\_and\_extract, the remainder is shifted left by 1 bit. Then the  $31^{st}$  bit of the quotient (\$s1) is put into the  $0^{th}$  bit position of the remainder (\$s3). The quotient is then shifted left by one bit. Next, an intermediate value (S) is calculated by subtracting the dvsr from the remainder. I was not able to call the actual sub\_logical routine since that will always jump back to the caller code, so I copy and pasted by sub\_logical code into this method. The difference is taken and is stored into S (\$v0). Next, we check if S is 0, basically if the Dvsr is greater than the remainder. If it is less than 0, we jump to increment counter. If S is not greater than 0 , we set R to equal S and make the  $0^{th}$  bit of Q a 1. Then we jump to increment counter and do the same checking.

#### *iv) increment counter*

Increment\_counter increments the counter by 1 and compares it to 32. If the counter equals 32, we jump to end\_division, or else we go back to left\_shift\_and\_extract.

#### *v)* end\_division

End\_division takes care of adding the proper sign to the quotient and remainder. The  $31^{st}$  bits of the original inputs are extracted and XOR is called on both of them. If the XOR is 1, that means only one number is negative, meaning that the sign bit should be negative. If the XOR'd answer is equal to 0, we branch to positive\_div. If it equals 1, we figure out the correct signs to put on the remainder and the quotient by using various twos complements calls.

#find twos compliment of rev

*vi) positive\_div* 

Positive div restores the stack and returns to the caller.

# IV. TESTING

Another class, called "proj\_alu\_normal" is created. This is also an arithmetic calculator, but does not use logic to perform the operations. Instead, it uses MIPS inbuilt arithmetic operations such as "add", "sub", "mul", and "div".

#### A) Implementation

# 1) addition au normal

Addition\_au\_normal calls the MIPS add instruction to add the two inputs. Just like in au\_logical, the arguments are passed through the method in a0 and a1, and the result is stored in v0.

# 2) subtraction au normal

Subtraction\_au\_normal calls the MIPS subtraction instruction to subtract the two inputs. Similarly to addition\_au\_normal, the arguments are passed through the method in \$a0 and \$a1, and the result is stored in \$v0.

# 3) Multiplication\_au\_normal

Multiplication\_au\_normal calls the MIPS "mul" instruction and stores the result in \$v0. The hi value is then moved into the \$v1 register.

## 4) Division au normal

Division\_au\_normal calls the MIPS "div" instruction on a0 and a1, which are the two inputs. The hi value contains the remainder and the lo value contains the quotient. The remainder is moved into v1 and the quotient is moved into v0.

#### *B) Proj-auto-test*

Professor Patra wrote assembly code which tests that the calculator works properly. The code provides sample inputs and does the operations using the au\_normal and au\_logical. The file see's if the au\_normal results match the au\_logical results. The following is a picture of the proj\_auto\_test

output.
---------

1		
(4 + 2)	normal => 6 logical => 6 [matched]	
(4 - 2)	normal => 2 logical => 2 [matched]	
(4 * 2)	normal => HI:0 LO:8 logical => HI:0 LO:8 [matched]	
(4 / 2)	normal => R:0 Q:2 logical => R:0 Q:2 [matched]	
(16 + -3)	normal => 13 logical => 13 [matched]	
(163)	normal => 19 logical => 19 [matched]	
(16 * -3)	normal => HI:-1 L0:-48 logical => HI:-1 L0:-48	[matched]
(16 / -3)	normal => R:1 Q:-5 logical => R:1 Q:-5 [matched]	
(-13 + 5)	normal => -8 logical => -8 [matched]	
(-13 - 5)	normal => -18 logical => -18 [matched]	
(-13 * 5)	normal => HI:-1 L0:-65 logical => HI:-1 L0:-65	[matched]
(-13 / 5)	normal => R:-3 Q:-2 logical => R:-3 Q:-2 [matched]	
(-2 + -8)	normal => -10 logical => -10 [matched]	
(-28)	normal => 6 logical => 6 [matched]	
(-2 * -8)	normal => HI:0 L0:16 logical => HI:0 L0:16 [matched]	
(-2 / -8)	normal => R:-2 0:0 logical => R:-2 0:0 [matched]	
(-6 + -6)	normal => -12 logical => -12 [matched]	
(-66)	normal => 0 logical => 0 [matched]	
(-6 * -6)	normal => HI:0 L0:36 logical => HI:0 L0:36 [matched]	
(-6 / -6)	normal => R:0 Q:1 logical => R:0 Q:1 [matched]	
(-18 + 18)	normal => 0 logical => 0 [matched]	
(-18 - 18)	normal => -36 logical => -36 [matched]	
(-18 * 18)	normal => HI:-1 L0:-324 logical => HI:-1 L0:-324	[matched]
(-18 / 18)	normal => R:0 Q:-1 logical => R:0 Q:-1 [matched]	
(5 + -8)	normal => -3 logical => -3 [matched]	
(58)	normal => 13 logical => 13 [matched]	
(5 * -8)	normal => HI:-1 L0:-40 logical => HI:-1 L0:-40	[matched]
(5 / -8)	normal => R:5 Q:0 logical => R:5 Q:0 [matched]	
(-19 + 3)	normal => -16 logical => -16 [matched]	
(-19 - 3)	normal => -22 logical => -22 [matched]	
(-19 * 3)	normal => HI:-1 L0:-57 logical => HI:-1 L0:-57	[matched]
(-19 / 3)	normal => R:-1 Q:-6 logical => R:-1 Q:-6 [matched]	
(4 + 3)	normal => 7 logical => 7 [matched]	
(4 - 3)	normal => 1 logical => 1 [matched]	
(4 * 3)	normal => HI:0 L0:12 logical => HI:0 L0:12 [matched]	
(4 / 3)	normal => R:1 Q:1 logical => R:1 Q:1 [matched]	
(-26 + -64)	normal => -90 logical => -90 [matched]	
(-2664)	normal => 38 logical => 38 [matched]	
$(-26 \times -64)$	normal => HI:0 L0:1664 logical => HI:0 L0:1664	[matched]
(-26 / -64)	normal => R:-26 Q:0 logical => R:-26 Q:0 [matched]	[marched]
(-20 / -04)	normal -> Ki-20 Qi0 (Ogical => Ki-20 Qi0 (Matched)	

Total passed 40 / 40 \*\*\* OVERALL RESULT PASS \*\*\*

-- program is finished running --

### V. CONCLUSION

This project, although a tough and tedious one, was made to implement a calculator using logical operations only. It was basically writing software that simulates the hardware, which performs these logical operations. The program was written in the MIPS assembly language and tested using a tester file that Professor Patra provided.